(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 369 773 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **89311832.3**

(51) Int. Cl.5: **G06F 5/06, G06F 13/18**

(22) Date of filing: **15.11.89**

(30) Priority: **16.11.88 JP 289222/88**

(43) Date of publication of application:
23.05.90 Bulletin 90/21

(84) Designated Contracting States:
DE FR GB

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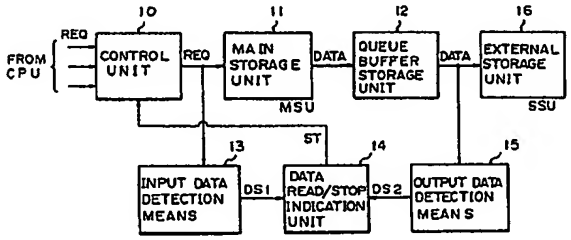
(54) Queue buffer memory control system.

(57) The queue buffer memory control system manages a busy state of data in a queue buffer memory (12) provided between a main storage unit (11) and an external storage unit (16). The queue buffer memory control system includes: a control unit (10) for receiving a request signal (REQ) from a central processing unit (CPU), selecting the priority order of the request signal (REQ) and decoding a destination command included in the request signal to determine whether or not the request signal indicates an access to the queue buffer memory (12); an output data detection unit (15) operatively connected to the queue buffer memory (12) for detecting the data quantity output from the queue buffer memory and outputting a detection signal at every detection of the data; an input data detection unit (13) operatively connected to an output side of the control unit (10) for detecting existence of data to be transferred to the queue buffer memory (12) based on the destination command of the request signal (REQ), and outputting a detection signal when the input data detection unit (13) detects the request signal before the main storage unit (11) receives the request signal; and a data read/stop indication unit (14) operatively connected to the input data detection unit (13) and the output data detection unit (15) for detecting the data quantity to be transferred to the queue buffer memory (12) based on the difference between the detection signals, and generating a stop signal to the control unit (10) for stopping an input of the request signal having the destination command of the data transfer from the main memory unit (11) to the queue buffer memory (12) when the data in the queue buffer memory (12) reaches a predetermined maximum quantity.

Fig. 2



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QUEUE BUFFER MEMORY CONTROL SYSTEM

The present invention relates to a queue buffer memory control system, more particularly, it relates to management of a busy state (busy management) of the queue buffer memory provided between a main storage unit and an external storage unit in a data processing system.

In a data processing system constituted by central processing units (CPU), main storage units (MSU), channel processors, and an external storage unit (SSU), a queue buffer memory is usually provided between the main storage unit and the external storage unit. In this case, only one external storage unit is provided in the multiprocessor system which is constituted by a plurality of clusters, each having central processing units, main storage units and channel processors.

When data is read out from the main storage unit and the data is also written into the external storage unit, the data is temporarily stored in the queue buffer memory and the data stored in the queue buffer memory is also written into the external storage unit. Accordingly, the queue buffer memory has a buffer function to solve an unbalanced state in which the read/write speed of the external storage unit is slower than that of the main storage unit so that these units operate asynchronously with each other.

In this case, there is a limit to the capacity of the queue buffer memory. Accordingly, it is necessary to effectively manage the busy state of queue buffer memory so that it is possible to raise the data transfer speed between the main storage unit and the external storage unit.

It is therefore desirable to provide queue buffer memory control system enabling effective management of the busy state of the queue buffer memory.

In accordance with the present invention, there is provided a queue buffer memory control system for managing the busy state of data at a queue buffer memory provided between a main storage unit and an external storage unit, including: a control unit for receiving a request signal from a central processing unit, selecting priority order of the request signal and decoding a destination command included in the request signal as to whether or not the request signal indicates an access to said queue buffer memory; an output data detection unit operatively connected to the queue buffer memory for detecting data quantity output from the queue buffer memory and outputting a detection signal at every detection of the data; an input data detection unit operatively connected to an output side of the control unit for detecting existence of data to be transferred to the queue buffer memory based on the destination command of the request signal, and outputting a detection signal when the input data detection unit detects the request signal before the main storage unit receives the request signal; and a data read/write indication unit operatively connected the input data detection unit and the output data detection unit for detecting the data quantity to be transferred to the queue buffer memory based on the difference between the detection signals, and generating a stop signal to send to the control unit for stopping input of the request signal having the destination command of the data transfer from the main memory unit to the queue buffer memory when the data quantity at the queue buffer memory has reached a predetermined maximum quantity.

Reference is made, by way of example, to the accompanying drawings in which:-

Fig. 1 is a schematic block of a queue buffer memory control system of an existing type;

Fig. 2 is a basic block diagram of queue buffer memory control system according to the present invention;

Fig. 3 is a schematic block diagram of a queue buffer memory control system according to an embodiment of the present invention; and

Fig. 4 is a detailed circuit diagram of the queue buffer memory control system shown in Fig. 3.

Before describing the preferred embodiments, an explanation will be given of problems of the present technology.

Fig. 1 is a schematic block diagram of a queue buffer memory control system of an existing type.

In Fig. 1, reference number 1 denotes a priority selection circuit, 2 a main memory, 3 a divider, 4 a queue buffer, 5 a busy state management circuit, 6 a queue buffer output control circuit, and 7 an external memory. Further, 21 to 26 denote registers, and 34 to 50 and 53 denote signal lines.

For example, when data is sequentially read out from the main memory 2 and written into the queue buffer 4, the data quantity exceeds the capacity of the queue buffer 4 If a write enabling signal is not generated from the external memory 7 to the queue buffer 4 and the queue buffer memory 4 cannot transfer the data to the external storage unit. Accordingly, it is necessary to provide the busy state management circuit 5 for controlling the data transfer between the main memory and the queue buffer.

The busy state management circuit 5 has the function of detecting the data quantity just stored in the queue buffer 4 based on the difference between the data quantity input from the main mem-

ory 2 to the queue buffer 4 and the data quantity output from the queue buffer 4 to the external memory 7. Further, the busy management circuit 5 has the function of outputting a busy signal for stopping a write request for writing the data into the queue buffer 4 when the data quantity at the queue buffer 4 reaches a predetermined limit of the capacity of the queue buffer memory. In this case, the limit of the capacity is determined by taking account of the data existing on the line between the main memory 2 and the queue buffer 4.

In general, several τ (τ: clock pulse period) are necessary as the transfer time from the reading out of the data at the main memory 2 until the writing of that data at the queue buffer 4. Assuming that the queue buffer 4 can store thirty-two blocks of data as the maximum capacity and that the transfer time is 20 τ, for example, in the state that the queue buffer 4 is completely filled by thirty two blocks of data, when the busy state management circuit 5 outputs the busy signal to stop the reading out of the data from the main memory 2, the data on the bus line between the main memory and the queue buffer (i.e., the data corresponding to the transfer time) are also written into the queue buffer 4.

Accordingly, as a countermeasure to the above problem, the busy state management circuit 5 outputs the busy signal at the timing when the data quantity reaches 12 data blocks (32 minus 20) as the predetermined limit of the capacity at the queue buffer 4. That is, the busy signal must be output at that timing by taking into account data existing on the line.

Therefore, there are problems in that a large useless capacity (area) occurs in the queue buffer 4 taking into account the data existing on the line. In this case, the busy signal must be frequently generated from the busy state management circuit 5 to effectively manage the state of the queue buffer 4 when the data quantity reaches the predetermined limit in spite of the existence of data on the line. Accordingly, these problems result in deterioration of the performance of the system.

Figure 2 is a basic block diagram of a queue buffer memory control system embodying the present invention.

In Fig. 2, reference number 10 denotes a control unit, 11 a main storage unit, 12 a queue buffer memory, 13 a input data detection unit, 14 a data read/stop indication unit, 15 an output data detection unit, and 16 an external storage unit.

The control unit 10 receives a request signal REQ from a central processing unit CPU and selects a priority order. The queue buffer memory 12 stores the data DATA read out from the main storage unit 11 which outputs the data after receiving a request signal REQ from the control unit 10. The output data detection unit 15 outputs a detection signal DS2 for each data input from the queue buffer memory 12. The input data detection unit 13 detects the request signal REQ before this signal REQ is input to the main storage unit 11 and outputs a detection signal DS1 indicating the data to be input to the main storage unit 11 at every detection of the request signal REQ.

The detection signals DS1 and DS2 are input to the data read/stop indication unit 14. The data read/stop indication unit 14 detects the data quantity to be stored in the queue buffer memory 12. The data read/stop indication unit 14 outputs a stop signal ST to the control unit 10 to stop the request signal REQ when the data quantity reaches the maximum quantity possible to store in the queue buffer memory 12. Accordingly, using the present invention, the data to be input to the queue buffer memory 12 can be detected in the previous stage read out from the main storage unit 11. Therefore, it is not necessary to take into account the data existing on the line between the main storage unit 11 and the queue buffer memory 12 and it is possible to effectively utilize the capacity of the queue buffer memory until reading a maximum state.

Figure 3 is a schematic block diagram of a queue buffer memory control system according to an embodiment of the present invention. In Fig. 3, reference number 1 denotes a priority selection circuit, 2 a main memory, 3 a dividing circuit, 4 a queue buffer, 5 a busy management circuit, 6 a queue buffer output control circuit, 21 to 26 registers, and 31 to 50 and 53 signal lines. In this embodiment, it is assumed that queue buffer 4 can store thirty two blocks of data as the maximum capacity.

The request signals REQ from the CPU's are transferred to the corresponding registers 21 to 23 through the signal lines 31 to 33. The priority selection circuit 1 selects the priority order of the request signal REQ output from each register through the signal lines 34 to 36. The priority selection circuit 1 outputs an access signal AC to the main memory 2 after determination of the priority order of the request signal REQ. The data stored in the main memory 2 is read out therefrom based on the access signal AC and transferred to the dividing circuit 3.

In the dividing circuit 3, the data is distributed to a corresponding register 24 to 26 in accordance with the kind of request, i.e., read request, write request and the like as shown in detail in Fig. 4. This is because the request signal includes a destination command indicating the destination of the data transfer. In case of the write request to the queue buffer 4 as the request made, the data is written into the queue buffer 4 through the register

24 and the signal line 43. Further, this data is also written into the external storage unit 7 through the signal line 48 under the predetermined conditions of the external storage unit 7.

That is, the queue buffer output control circuit 6 outputs an output enable signal OE to the queue buffer 4 through the signal line 53 and the data stored in the queue buffer 4 is output to the external storage unit 7 through the signal line 48 if a busy signal BS is not output from the external storage unit 7 through the signal line 49.

Further, the queue buffer output control circuit 6 outputs an information signal IS1 to the busy management circuit 5 to inform the fact that the data is output from the queue buffer 4 to the external storage unit 7. The information signal IS1 is output from the queue buffer output control circuit 6 every time the above operation is carried out.

The priority selection circuit 1 decodes each request signal REQ input from each register 21 to 23, and detects whether or not information indicating the data transfer from the main memory to the queue buffer 4 is included in the request signal REQ based on the destination command included therein. Further, the priority selection circuit 1 outputs an information signal IS2 to the busy management circuit 5. The information signal IS2 is output from the priority selection circuit 1 to the busy management circuit 5 at every detection of the destination command.

Accordingly, the information signals IS1 and IS2 are input to the busy management circuit 5. As explained above, the former is output from the queue buffer output control circuit 6 and the latter is output from the priority selection circuit 1. The busy management circuit 5 can detect the data quantity stored in the queue buffer 4 based on the difference between the information signals IS1 and IS2. Therefore, the busy management circuit 5 can output the busy signal BS to the priority selection circuit 1 when the data quantity reaches thirty two blocks of data in the queue buffer 4 based on the above calculation. When the priority selection circuit 1 receives the busy signal BS, the priority selection circuit 1 temporarily stops the request signal REQ to prevent writing data into the queue buffer 4 as shown in detail in Fig. 4.

Figure 4 is a detailed circuit diagram of the circuit shown in Fig. 3. As shown in this drawing, the priority selection circuit 1 comprises a priority selector 11, a pipe-line unit 12 and a decoder 13. The queue buffer 4 is preferably divided into two blocks 41 and 42 for discriminating whether the area in question is associated with a read operation or a write operation. In this case, the queue buffer output control circuit 6 in Fig. 3 is included in the block 42. The busy state management circuit 5 is mainly constituted by a counter 51 and a comparator 52.

The decoder 13 decodes the destination command included in each request signal REQ as to whether or not the destination command indicates the request of the data to be written into the external memory 7 through the main memory 2 and the queue buffer 42. The decoder 13 outputs the information signal IS2 to the counter 51 when the decoder 13 decodes such a request signal. As explained in Fig. 3, the information signal IS1 is output from the queue buffer output control circuit 6 and input to the counter 51 to count it down. The comparator 52 compares the information signal IS2 with the information signal IS2 based on the count value. Further, the comparator outputs a busy signal BS to the priority selector 11 when the count value exceeds the predetermined limit of the capacity of the queue buffer memory 4.

The pipe-line 12 is provided as a shift register for delaying the request signal. This delay is performed to coincide the transfer speed of the request signal with the read-out speed of the data from the main memory 2. Accordingly, the input timing of the request signal to the divider 3 is coincided with that of the read-out data to the divider 3. The divider 3 is provided for dividing the request signal in accordance with the destination command included in each request signal as explained above. When the request indicates an access of the queue buffer 42, the data is transferred from the main memory 2 to the queue buffer 42 through the signal line ④. Other destinations ① to ③ are returned to, for example, the CPU.

The external storage unit (SSU) 7 is provided for cluster management in the multiprocessor system. One external storage unit is connected in parallel to a plurality of clusters. However, the structure of the multiprocessor system is omitted to simplify the explanation of the present invention.

Claims

1. A queue buffer memory control system for managing a busy state of data in a queue buffer memory provided between a main storage unit and an external storage unit, comprising:

a control means (10) for receiving a request signal (REQ) from a central processing unit (CPU), selecting a priority order of said request signal and decoding a destination command included in said request signal to determine whether or not said request signal indicates an access to said queue buffer memory;

an output data detection means (15) operatively connected to said queue buffer memory (12) for detecting a data quantity output from said queue

buffer memory and outputting a detection signal (DS2) at every detection of said data;

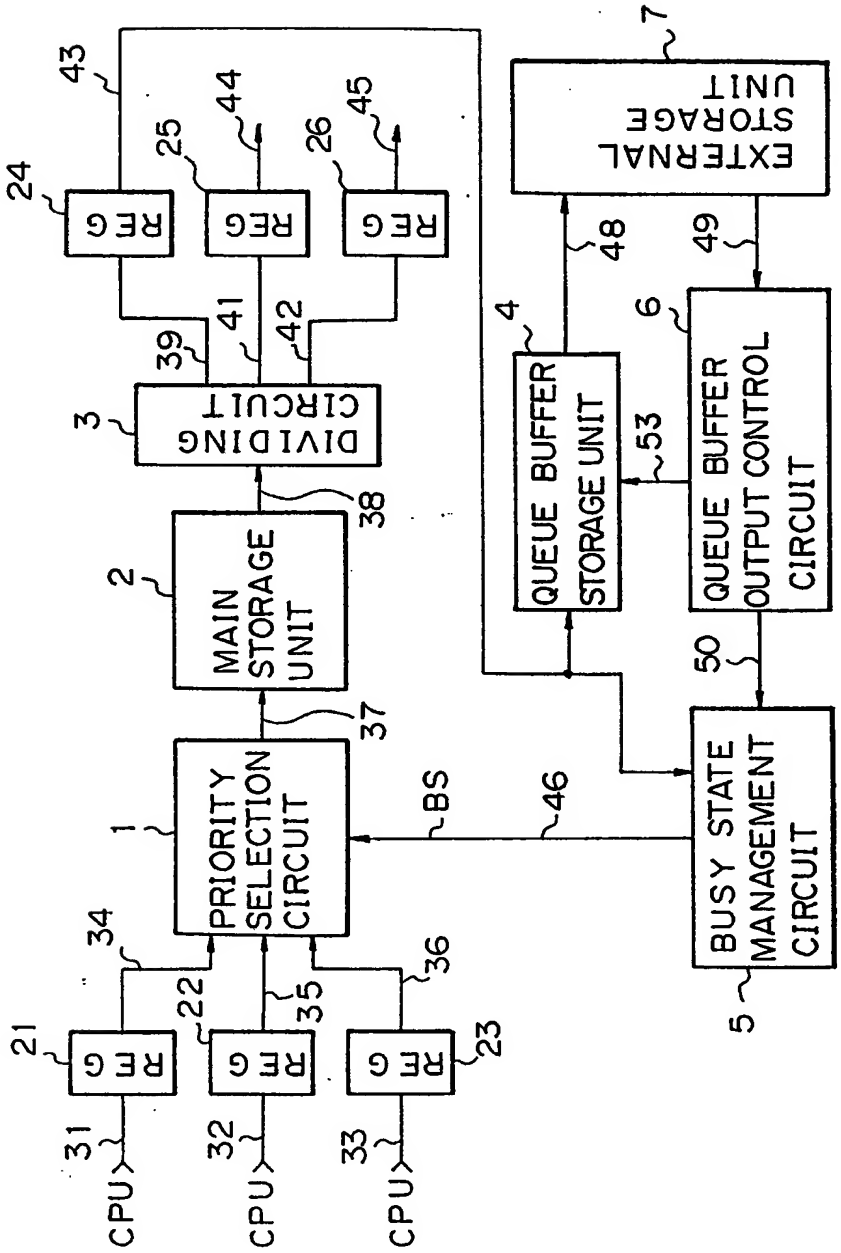
an input data detection means (13) operatively connected to an output side of said control means for detecting existence of data to be transferred to said queue buffer memory based on said destination command of said request signal, and outputting a detection signal (DS1) when said input data detection means detects said request signal before said main storage unit (11) receives said request signal; and

a data read/ stop indication means operatively connected to said input data detection means and said output data detection means for detecting the data quantity to be transferred to said queue buffer memory based on the difference between said detection signals (DS1, DS2), and generating a stop signal (ST) to said control means for stopping an input of said request signal having said destination command of the data transfer from said main memory unit to said queue buffer memory when the data quantity at said queue buffer memory reaches a predetermined maximum quantity.

2. A queue buffer memory control system as claimed in claim 1, wherein said control means comprises a priority selection circuit having a priority selector for selecting a priority order of said request signal, a pipe-line unit for delaying transfer of said request signal, and a decoder for decoding said destination command included in said request signal.

3. A queue buffer memory control system as claimed in claim 1 or 2, wherein said data read/stop indication means comprises a counter circuit for counting said information signals, and a comparator for comparing a count value of said information signal with that of the other information signal and outputting said busy signal to said priority selector when said counting value reaches a predetermined limit of the data capacity at said queue buffer memory.

Fig. 1


CPU
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REG
PRIORITY SELECTION CIRCUIT
MAIN STORAGE UNIT
DIVIDING CIRCUIT
QUEUE BUFFER STORAGE UNIT
QUEUE BUFFER OUTPUT CONTROL CIRCUIT
BUSY STATE MANAGEMENT CIRCUIT
EXTERNAL STORAGE UNIT
BS
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Fig. 2

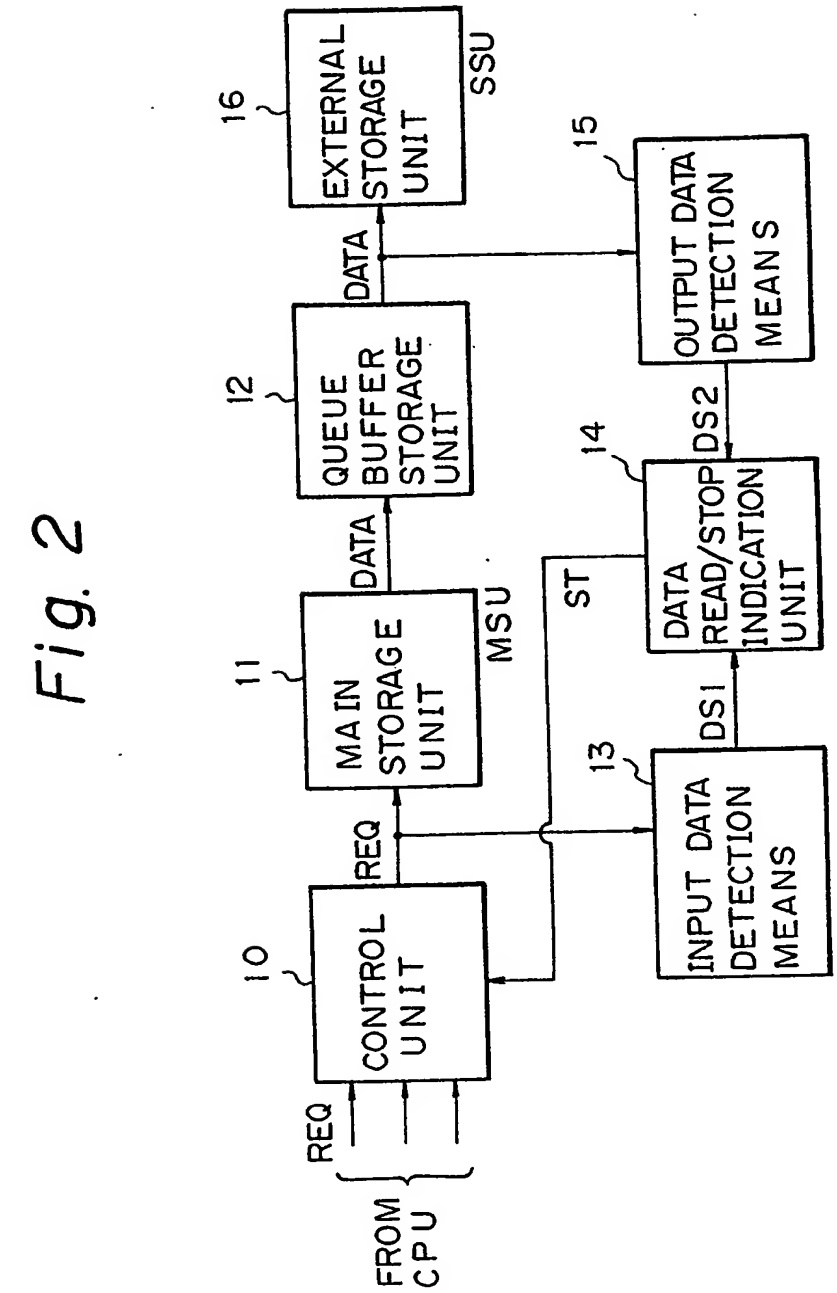
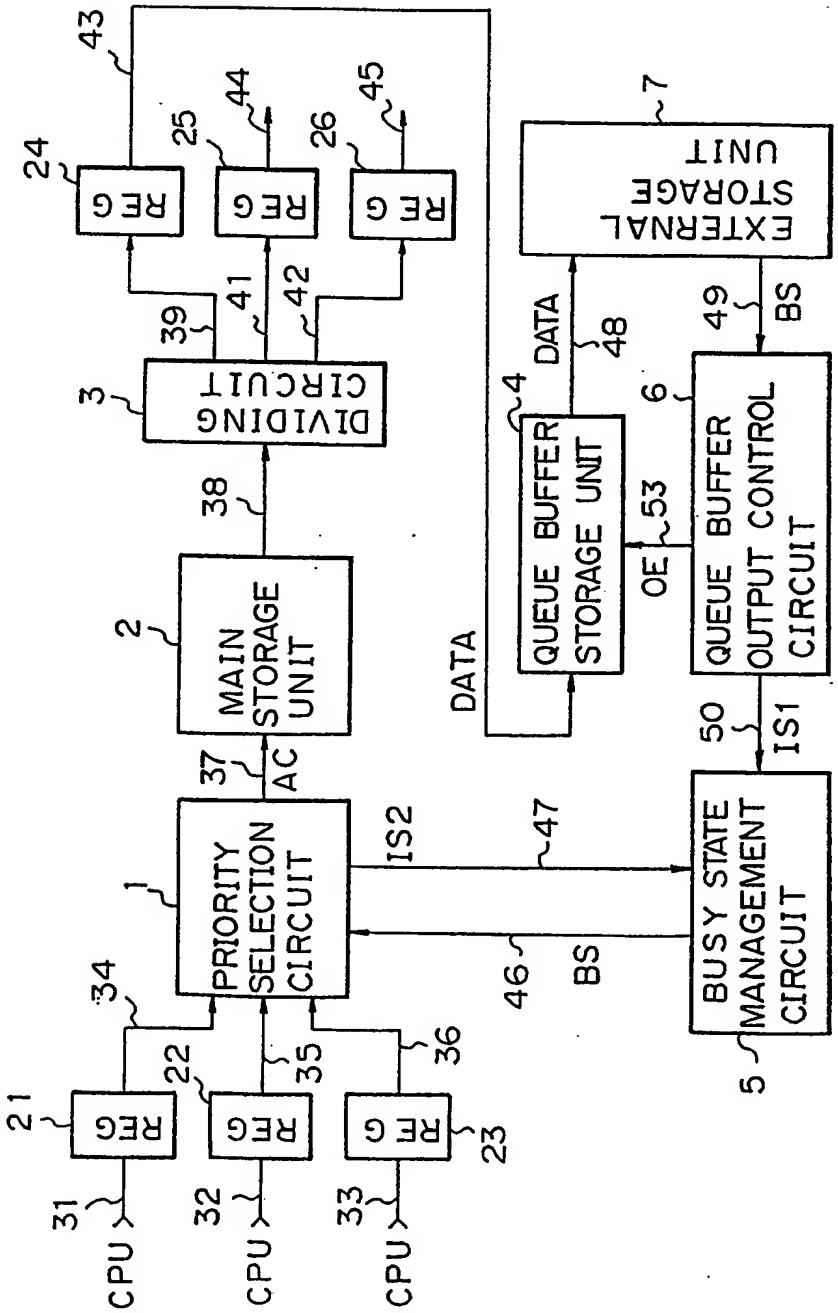

FROM CPU
REQ
10
CONTROL UNIT
REQ
11
MAIN STORAGE UNIT
MSU
DATA
12
QUEUE BUFFER STORAGE UNIT
DATA
16
EXTERNAL STORAGE UNIT
SSU
ST
13
INPUT DATA DETECTION MEANS
DS1
14
DATA READ/STOP INDICATION UNIT
DS2
15
OUTPUT DATA DETECTION MEANS

Fig. 3


CPU
CPU
CPU
REG
REG
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REG
PRIORITY SELECTION CIRCUIT
MAIN STORAGE UNIT
DIVIDING CIRCUIT
QUEUE BUFFER STORAGE UNIT
QUEUE BUFFER OUTPUT CONTROL CIRCUIT
BUSY STATE MANAGEMENT CIRCUIT
EXTERNAL STORAGE UNIT
DATA
DATA
AC
IS1
IS2
BS
BS
OE
1
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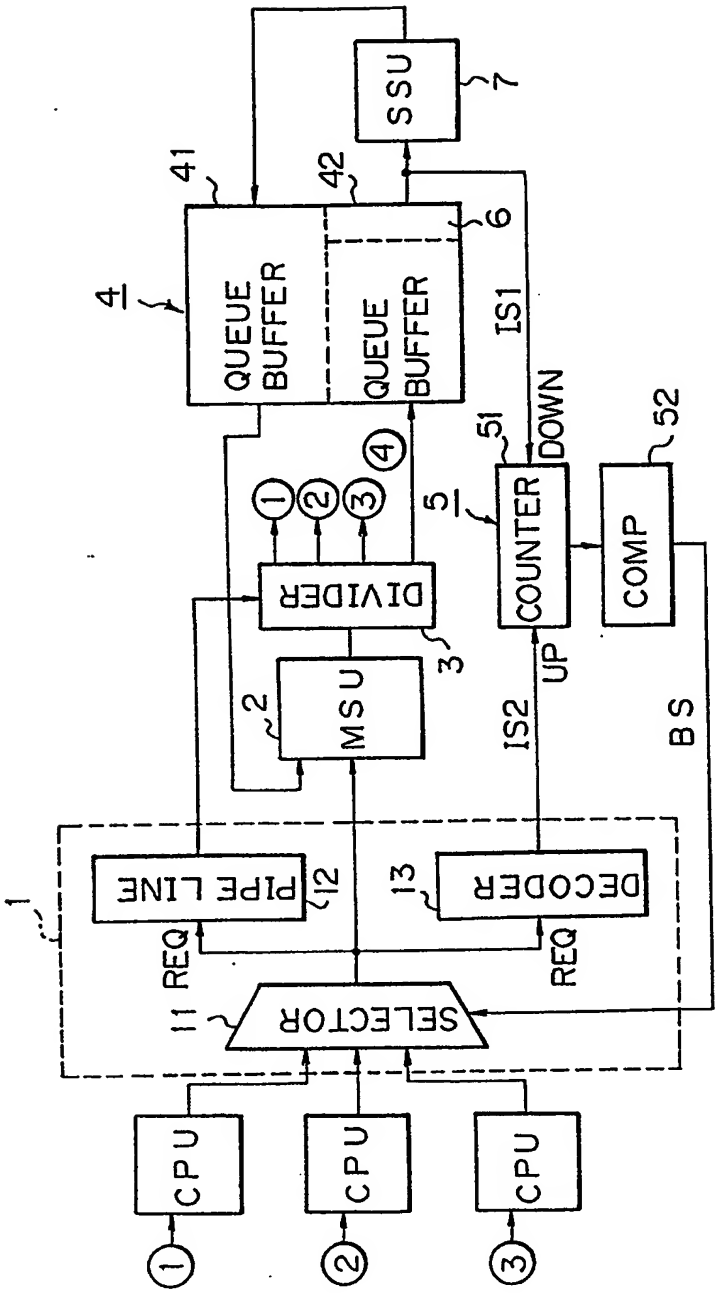
Fig. 4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QUEUE BUFFER
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DOWN
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52
5
COUNTER
COMP
DIVIDER
3
MSU
2
IS2
UP
BS
PIPE LINE
12
13
DECODER
1
REQ
REQ
11
SELECTOR
CPU
CPU
CPU
1
2
3
4